What is claimed is:

1. The process for the manufacture of a substrate for a superjunction device, said process comprising the steps of: forming a first epitaxial semiconductor layer of a given thickness and of a given impurity concentration of a first conductivity type atop a support body forming a plurality of spaced implants of a second conductivity type on the surface of said first epitaxial layer; forming a second epitaxial layer of a given thickness and of a given concentration and of said first conductivity type atop said first layer; and thereafter heating said substrate and said implants to cause said implants to diffuse downwardly into said first layer and upwardly into said second layer, thereby forming spaced pedestals of said second conductivity type within said first and second layers; the total charge of each of said pedestals being approximately equal to the total charge in the volume of said first and second layers which surrounds said pedestals.

2. The process of claim 1, in which said first and second layers are silicon.

3. The process of claim 1, wherein said first and second layers are of the same thickness and impurity concentration.

4. The process of claim 2, wherein said support body is a silicon wafer.

5. The process of claim 4, wherein said first and second layers are of the same thickness and concentration.

6. The process of claim 4, wherein said silicon wafer has the same conductivity type as said first and second layers.

7. The process for the manufacture of a superjunction device comprising the steps of: forming a first epitaxial semiconductor layer of a given thickness and of a given impurity concentration of a first conductivity type atop a support body; forming a plurality of spaced implants of a second conductivity type on the surface of said first epitaxial layer; forming a second epitaxial layer of a given thickness and of a given concentration and of said first concentration type atop said first layer; heating said substrate and said implants to cause said implants to diffuse downwardly into said first layer and upwardly into said second layer, thereby forming spaced pedestals of said second conductivity type within said first and second layers; the total charge of each of said pedestals being approximately equal to the total charge of the volume of said first and second layers which surrounds said pedestals; and thereafter forming MOSgated cell elements atop each of said pedestals.

8. The process of claim 7, which further includes forming a drain electrode on the bottom of said support layer, and separating said support layer and said MOSgated cell elements into separate unitary elements.

9. The process of claim 7, wherein said support body is a silicon wafer.

10. The process of claim 9, wherein said silicon wafer has the same conductivity type as said first and second layers.

11. The process of manufacture of a substrate wafer for the manufacture of superjunction devices, comprising the steps of depositing an epitaxial layer of semiconductor material of one conductivity type atop a support wafer; forming a plurality of laterally spaced implants of the second conductivity type at vertically interior locations of said epitaxial layer; and thermally diffusing said implants to cause them to diffuse for a given distance upwardly and downwardly within said epitaxial layer, thereby to form laterally spaced superjunction pedestals within said epitaxial layer; the total charge of said second conductivity type within each of said

pedestals being at least approximately matched to the total charge of the first conductivity type of said epitaxial layers which surrounds each of said pedestals.

12. The process of claim 11, wherein said implants are formed at the approximate mid-point of the thickness of said epitaxial layer.

13. The process of claim 12, wherein said epitaxial layer consists of first and second sequentially formed layers.

14. The process of claim 11, wherein said epitaxial layer and said support wafer are silicon.

15. The process of claim 12, wherein said epitaxial layer and said support wafer are silicon.

16. The process of claim 13, wherein said epitaxial layer and said support wafer are silicon.

17. The process for the manufacture of a semiconductor device which includes the steps of depositing an epitaxial layer of semiconductor material of one conductivity type atop a support wafer; forming a plurality of laterally spaced implants of the second conductivity type at vertically interior locations of said epitaxial layer; and thermally diffusing said implants to cause them to diffuse for a given distance upwardly and downwardly within said epitaxial layer, thereby to form laterally spaced superjunction pedestals within said epitaxial layer; the total charge of said second conductivity type within each of said pedestals being at least approximately matched to the total charge of the first conductivity of said epitaxial layers which surrounds each of said pedestals and thereafter forming MOSgated cell elements atop each of said cell elements.